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10/580,467	05/25/2006	Yoshitaka Ohta	2006_0752A	4360

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EXAMINER	
BEYEN, ZEWDU A	

ART UNIT	PAPER NUMBER
4144	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/580,467	OHTA ET AL.	
	Examiner	Art Unit	
	ZEWDU BEYEN	4144	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05/25/2006* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/25/2006*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. claims1-13, have been examined and are pending.

Information Disclosure Statement

2. An initialed and dated copy of applicant's IDS form 1449 submitted 05/25/2006, is attached to the instant office action.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims1-3, and , 9-13 are rejected under 35 U.S.C. 103(a) as being unpatentable over applicant admitted prior art ("AAPA") , and further in view of Yamada to (US6675314)

Regarding claims 1, and 13, AAPA teaches a data reception device for receiving a data packet

containing a plurality of packets, wherein first time information regarding time at which the plurality of packets are generated is added to each of the plurality of packets, the data reception device comprising **(figs. 12, [0004], and [0005] disclose receiving plurality of packets by wireless device)**:

a receive data buffer unit **(fig.12 box.933)** for storing the plurality of packets contained in the data packet**([0008] discloses storing the received data block);**

a time information output unit for outputting**(fig.12 box 926)** second time information **(i.e. current time)** counted in accordance with a frequency of the clock generated by the variable clock generation unit**(fig.12 box.928) ([0009] discloses based on clock outputted from the clock generation unit , the beacon timer unit sets a current timer value)** ;

a first time information comparison unit **(fig.12 box.931)** for comparing the first time information added to the plurality of packets with the second time information outputted from the time information output unit and for controlling timing of outputting the plurality of the packets stored in the receive data buffer unit**([0010] discloses a PLL processing unit 929 performs PLL processing for the timer value from the beacon timer unit 926 and inputs the processed timer value to a timer unit 930. The timer unit 930 inputs the current timer value, for which the PLL processing has been performed, to a time stamp comparison unit 931. A time stamp extraction unit 932 extracts a time stamp contained in a data block which has been stored in the receive data buffer unit 933. The time stamp**

comparison unit 931 determines whether or not the timer value contained in the time stamp which the time stamp extraction unit 932 has extracted and the current timer value inputted from the timer unit 930 match with each other)

AAPA silent on a variable clock generation unit for generating a clock whose frequency is variable; wherein the receive data amount measuring unit controls a frequency of the clock generated by the variable clock generation unit in accordance with values measured by the receive data amount measuring unit; a receive data amount measuring unit for measuring a data amount stored in the receive data buffer unit;

However, Yamada teaches a variable clock generation unit **(fig.1 box. 23)** for generating a clock whose frequency is variable **(col.4 lines 25-35 discloses a buffer-remaining volume monitoring section 12 obtains a buffer remaining volume H from a write signal and a read signal to the source clock regeneration buffer 23, and monitors this buffer remaining volume H. A control-voltage calculating section 1 calculates a control voltage V to a voltage control crystal oscillator 13 based on the buffer remaining volume H output from the buffer-remaining volume monitoring section 12. The voltage control crystal oscillator (VCXO) 13 changes an oscillation frequency (local clock 44) according to the control voltage V from the control-voltage calculating section 1, thus resulted variable frequencies);**

a receive data amount measuring unit **(Yamada, fig.1 box.12)** for measuring a data amount stored in the receive data buffer unit**(Yamada, abstract discloses the buffer remaining volume monitoring section monitors the amount of the data left in the received buffe**r) ;

wherein the receive data amount measuring unit controls a frequency of the clock generated by the variable clock generation unit in accordance with values measured by the receive data amount measuring unit **(Yamada,col.4 lines 19-35, FIG. 19 disclose structure of the AAL processing section 20. In this AAL processing section 20, a source clock regeneration buffer 23 temporarily holds a reception cell. A source clock regenerating section regenerates the source clock. A buffer control section 11 controls the reading from the source clock regeneration buffer 23. A buffer-remaining volume monitoring section 12 obtains a buffer remaining volume H from a write signal and a read signal to the source clock regeneration buffer 23, and monitors this buffer remaining volume H. A control-voltage calculating section 1 calculates a control voltage V to a voltage control crystal oscillator 13 based on the buffer remaining volume H output from the buffer-remaining volume monitoring section 12. The voltage control crystal oscillator (VCXO) 13 changes an oscillation frequency (local clock 44) according to the control voltage V from the control-voltage calculating section 1).**

Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to include variable clock generation unit for generating a clock whose frequency is variable , a receive data amount measuring unit for measuring a data amount

stored in the receive data buffer unit and wherein the receive data amount measuring unit controls a frequency of the clock generated by the variable clock generation unit in accordance with values measured by the receive data amount measuring unit, as suggested by Yamada. This modification would benefit the system of AAPA to render the received data smoothly and improve the quality.

Regarding claim 2, the combination of AAPA- Yamada teaches the data reception device according to claim 1, wherein the second time information outputted by the time information comparison unit is delayed by a predetermined offset time **(i.e. fluctuation time) (AAPA, [0013] discloses a fluctuation time (25 microsecond or less) between the time on the transmitted packets and the actual time the packets are received at the receiving side).**

Regarding claim 3, the combination of AAPA- Yamada teaches the data reception device according to claim 2, wherein the time information output unit comprises:
a timer unit for outputting third time information **(i.e. the updated current timer value)** counted in accordance with a frequency of the clock generated by the variable clock generation unit**(AAPA, [0009] discloses the beacon timer unit 926 updates the current timer values so that the current timer value and the timer value contained in the beacon signal in the received packets match) :**

a time information extraction unit for extracting the first time information added to the plurality of packets stored in the receive data buffer unit(**AAPA, [0010] discloses a time stamp extraction unit 932 extracts a time stamp contained in a data block which has been stored in the receiving buffer unit 933) ;**

an initialization unit for coinciding the third time information outputted by the timer unit with the first time information extracted by the time information extraction unit **(AAPA, [0009] discloses the beacon timer unit 926 updates the current timer values so that the current timer value and the timer value contained in the beacon signal in the received packets match)**;
an offset unit for outputting the second time information by delaying(**AAPA, [0013] discloses reproducing system clock which has a fluctuation value)** , by the predetermined offset time **(i.e. 25 microsecond or less)** , the third time information **(i.e. the updated current timer value)** outputted by the timer unit(AAPA, **[0009] discloses the beacon timer unit 926 updates the current timer values).**

Regarding 9, the combination of AAPA- Yamada teaches the data reception device according to claim 3, wherein after a predetermined time has passed, the receive data amount measuring unit starts controlling a frequency of the clock generated by the variable clock generation unit after predetermined time has passed**(Yamada, col.10 lines 25-34 discloses the control unit has a timer for counting a pre-decided duration of time and the predetermined condition is a lapse of the constant time counted by the timer, when a constant time counted by the timer**

passed , and a clock regeneration control of high frequency stability is carried out by the lapse of this constant time)

Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to include wherein after a predetermined time has passed, the receive data amount measuring unit starts controlling a frequency of the clock generated by the variable clock generation unit after predetermined time has passed, as suggested by Yamada. This modification would benefit the system of the combination to render the received data smoothly and improve the quality.

Regarding 10, the combination of AAPA- Yamada teaches the data reception device according to claim 1, wherein the receive data amount measuring unit controls the frequency of the clock generated by the variable clock generation unit by using an average value, as a measured value, of data amounts accumulated in the receive data buffer unit **(Yamada, (US6675314), col. 9 lns 26-30 and col.4 lns 19-35 disclose a buffer control section 11 controls the reading from the source clock regeneration buffer 23. A buffer-remaining volume monitoring section 12 obtains a buffer remaining volume H from a write signal and a read signal to the source clock regeneration buffer 23, and monitors this buffer remaining volume H. A control-voltage calculating section 1 calculates a control voltage V to a voltage control crystal oscillator 13 based on the buffer remaining volume H output from the buffer-remaining volume monitoring section 12. The voltage control crystal oscillator (VCXO) 13 changes an**

oscillation frequency (local clock 44) according to the control voltage V from the control-voltage calculating section 1).

Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to include wherein the receive data amount measuring unit controls the frequency of the clock generated by the variable clock generation unit by using an average value, as a measured value, of data amounts accumulated in the receive data buffer unit, as suggested by Yamada. This modification would benefit the system of the combination to render the received data smoothly and improve the quality.

Regarding 11, the combination of AAPA- Yamada teaches the data reception device according to claim 1, wherein the plurality of packets contained in the data packet are MPEG2-TS packets **(AAPA, [0004] discloses MPEG2-TS packets).**

Regarding 12, the combination of AAPA- Yamada teaches the data reception device according to claim 1, wherein as the data packet, audio signals and video signals are encoded to be generated as a plurality of MPEG2-TS packets to each of which first time information regarding time at encoding time is added, and the plurality of MPEG2-TS packets having the added first time information are combined and transmitted from the data transmission device which is operable to generate the data packet **(AAPA, [0004] discloses video signal inputted to an MPEG2-TS encoding unit are converted to an MPEG2-TS packet and outputted. A time**

stamp addition unit adds to the MPEG2-TS packet a time stamp in accordance with time at which the MPEG2-TS packet is outputted from the MPEG2-TS encoding unit).

4. Claims 7 and 8 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA , and Yamada to **(US6675314)** as applied in claim 1 above **and further in view of** Woodhead to **(US5640388).**

Regarding 7, the combination of AAPA- Yamada silent on the data reception device according to claim 3, comprising a second time information comparison unit for comparing the third time information outputted by the timer unit with the first time information extracted by the time information extraction unit and for controlling, based on a comparison result, a frequency of the clock generated by the variable clock generation unit

However, Woodhead teaches a second time information comparison unit for comparing the third time information outputted by the timer unit with the first time information extracted by the time information extraction unit and for controlling, based on a comparison result, a frequency of the clock generated by the variable clock generation unit **(,Woodhead,col.5 lns 40-51, discloses subtractor compares the counter value with subsequent PCRs as they arrive in the transport stream packets. since a PCR when it arrives represents the expected value of the decoder system clock at the time that PCR is received , the**

difference between it and the value of counter used to drive the frequency of the VCO to adjust the decoder clock).

Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to include a second time information comparison unit for comparing the third time information outputted by the timer unit with the first time information extracted by the time information extraction unit and for controlling, based on a comparison result, a frequency of the clock generated by the variable clock generation unit, as suggested by Woodhead. This modification would benefit the system of the combination to render the received data smoothly and improve the quality.

Regarding 8. the combination of AAPA- Yamada-Woodhead teaches the data reception device according to claim 7, wherein until a predetermined time from a time point of starting reception of the data packet has passed, a frequency of the clock generated by the variable clock generation unit is controlled by the second time information comparison unit**(Woodhead,col.5 lns 40-51, discloses subtractor compares the counter value with subsequent PCRs as they arrive in the transport stream packets. since a PCR when it arrives represents the expected value of the decoder system clock at the time that PCR is received, the difference between it and the value of counter used to drive the frequency of the VCO to adjust the decoder clock).** and after the predetermined time from the time point of starting reception of the data packet has passed, the frequency of the clock generated by the variable clock generation unit is controlled by the receive data amount measuring unit**(Yamada, col.10 lns 25-34 discloses the control unit has a timer for counting a pre-decided duration of time and the predetermined condition is**

a lapse of the constant time counted by the timer, when a constant time counted by the timer passed , and a clock regeneration control of high frequency stability is carried out by the lapse of this constant time).

Therefore it would have been obvious to one ordinary skill in the art at the time the invention was made to include wherein until a predetermined time from a time point of starting reception of the data packet has passed, a frequency of the clock generated by the variable clock generation unit is controlled by the second time information comparison unit, as suggested by Woodhead and after the predetermined time from the time point of starting reception of the data packet has passed, the frequency of the clock generated by the variable clock generation unit is controlled by the receive data amount measuring unit, as suggested by Yamada . This modification would benefit the system of the combination to render the received data smoothly and improve the quality.

5. Claims 4-6 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA, and Yamada to **(US6675314)** as applied in claim 1 above **and further in view of** below.

Regarding 4, the combination of AAPA- Yamada silent on the data reception device according to claim 3, wherein the offset unit changes the predetermined offset time in accordance with conditions of a transmission line where the data reception device is connected.

However, it would have been obvious to one ordinary skill in the art at the time the invention was made to include the offset unit changes the predetermined offset time in accordance with conditions of a transmission line where the data reception device is connected. It is obvious that wireless connection faster than wire line connection, so to compensate the speed difference, adjusting the offset value according to the connection line is an obvious measure for rendering the received packets smoothly.

Regarding 5, the combination of AAPA- Yamada silent on the data reception device according to claim 3, wherein the offset unit changes the predetermined offset time in accordance with a data amount accumulated in the receive data buffer unit.

However, it would have been obvious to one ordinary skill in the art at the time the invention was made to include the offset unit changes the predetermined offset time in accordance with a data amount accumulated in the receive data buffer unit. To avoid over flow and under flow in the receive data buffer unit, adjusting the offset value according data amount accumulated in the receive data buffer unit is an obvious measure for rendering the received packets smoothly.

Regarding 6, the combination of AAPA- Yamada silent on the data reception device according to claim 3, wherein the offset unit changes the predetermined offset time in accordance with a kind of a communication protocol.

However, it would have been obvious to one ordinary skill in the art at the time the invention was made to include the offset unit changes the predetermined offset time in accordance with a kind of a communication protocol. Different communication protocols have different congestion level and different amount of packets that carried during communication. So, to facilitate smooth rendering and improve the continuity of the packets flow, adjusting the offset value according to communication protocol is an obvious measure

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

US Patent Application Publication No. 2005/0117583 A1 to Uchida et al. discloses Method and apparatus for receiving packets transmitted from transmission apparatus

US Patent Application Publication No. 2005/0237937 A1 to Gestel discloses Jitter compensation method for systems having wall clocks

US Patent No.7362838 B2 to Mizukaml et al. discloses Synchronization method and system, and decoder

US Patent No.6404711 B1 to Kato discloses System including comparing a separated time stamp to a generated timing signal and controlling a timing signal on the basis of continuity of time stamps

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zewdu Beyen whose telephone number is (571)-270-7157. The examiner can normally be reached on 8:00-5:30 Mon-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Taghi T. Arani can be reached on (571) 272-3787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/ZEWDU BEYEN/

Examiner, Art Unit 4144

/Taghi T. Arani/

Supervisory Patent Examiner, Art Unit 4144